CLAIMS

We claim:

sub-a1

1. A method of packet processing comprising:

parsing a packet, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data;

searching one or more data structures based on said header data to produce search results;

editing said packet based on said search results, said header data, and said vector;

wherein said coordinating further comprises monitoring said deconstructing, said searching, and said editing.

2. The method of Claim 1, wherein said coordinating further comprises sharing data with said parsing, said deconstructing, said searching, and said editing.

3. The method of Claim 1, further comprising buffering said packet before said parsing.

4. The method of Claim 1, wherein:

said deconstructing further comprises forming a search argument; and

said searching uses said search argument.

5. The method of Claim 1, wherein:

said deconstructing further comprises forming a search argument;

said coordinating further comprises operating on said search argument to form a modified search argument prior to said searching; and

said searching uses said modified search argument.

6. An apparatus for packet processing, comprising:

a central processor for packet processing, said central processor comprising a register set; and

one or more peripheral processors each connected to said central processor and each comprising a register set, wherein each said peripheral processor returns at least one datum to said central processor;

wherein said central processor communicates with each said peripheral processor.

7. The apparatus of Claim 6, wherein said central processor comprises a general purpose processor.

8. The apparatus of Claim 6, wherein said central processor comprises a microsequencer.

9. The apparatus of Claim 6, wherein said central processor comprises more than one processor acting in concert.

10. The apparatus of Claim 6, wherein one or more of said peripheral processors comprise fixed logic circuits.

11. The apparatus of Claim 6, wherein one or more of said peripheral processors comprise programmable logic circuits.

12. The apparatus of Claim 6, wherein one or more of said peripheral processors comprise a programmable state machine.

13. The apparatus of Claim 6, wherein a portion of each said peripheral register set is mapped onto said central processor register set.

14. The apparatus of Claim 6, wherein said central processor and at least one peripheral processor together form at least a part of a single application specific integrated circuit.

15. A computer system for packet processing, comprising computer instructions for:

parsing a packet, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data;

searching one or more data structures based on said header data to produce search results;

editing said packet based on said search results, said header data, and said vector;

wherein said coordinating further comprises monitoring said deconstructing, said searching, and said editing.

16. The computer system of Claim 15, wherein said coordinating further comprises sharing data with said parsing, said deconstructing, said searching, and said editing.

17. The computer system of Claim 15, further comprising buffering said packet before said parsing.

18. The computer system of Claim 15, wherein:

said deconstructing further comprises forming a search argument; and

said searching uses said search argument.

19. The computer system of Claim 15, wherein:

said deconstructing further comprises forming a search argument;

said coordinating further comprises operating on said search argument to form a modified search argument prior to said searching; and

said searching uses said modified search argument.

20. A computer-readable storage medium, comprising computer instructions for:

parsing a packet, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data;

searching one or more data structures based on said header data to produce search results;

editing said packet based on said search results, said header data, and said vector;

wherein said coordinating further comprises monitoring said deconstructing, said searching, and said editing.

21. The computer-readable storage medium of Claim 20, wherein said coordinating further comprises sharing data with said parsing, said deconstructing, said searching, and said editing.

22. The computer-readable storage medium of Claim 20, further comprising buffering said packet before said parsing.

23. The computer-readable storage medium of Claim 20, wherein:

said deconstructing further comprises forming a search argument; and

said searching uses said search argument.

24. The computer-readable storage medium of Claim 20, wherein:

said deconstructing further comprises forming a search argument;

said coordinating further comprises operating on said search argument to form a modified search argument prior to said searching; and

said searching uses said modified search argument.

25. A computer data signal embodied in a carrier wave, comprising computer instructions for:

parsing a packet, said packet having a header portion, to determine a vector;

coordinating processing using said vector;

deconstructing said packet header to form header data;

searching one or more data structures based on said header data to produce search results;

editing said packet based on said search results, said header data, and said vector;

wherein said coordinating further comprises monitoring said deconstructing, said searching, and said editing.

26. The computer data signal of Claim 25, wherein said coordinating further comprises sharing data with said parsing, said deconstructing, said searching, and said editing.

27. The computer data signal of Claim 25, further comprising buffering said packet before said parsing.

28. The computer data signal of Claim 25, wherein:

said deconstructing further comprises forming a search argument; and

said searching uses said search argument.

29. The computer data signal of Claim 25, wherein:

said deconstructing further comprises forming a search argument;

said coordinating further comprises operating on said search argument to form a modified search argument prior to said searching; and

said searching uses said modified search argument.